ABSTRACT OF THE DISCLOSURE

An apparatus for verifying memory coherency of a duplication processor having a symmetrical structure includes: an active processor in which a standby memory read command (SMRC) is generated and transmitted by hardware and then a read data of the standby memory which has been inputted corresponding to the SMRC is image-buffered to verify a memory coherency; and a standby processor in which the SMRC transmitted from the active processor is analyzed and a read command of a standby memory is outputted, and then the data read from the standby memory is transmitted to the active processor. A burst transaction can be performed both when the data is read from the standby memory and when the read data is transmitted, so that the use efficiency of the processor bus, the duplication bus and the duplication channel can be improved. Especially, a bad influence according to the operation of each processor and the duplication channel can be minimized. Moreover, the SMIB provides burst mechanism function, so that the CPU of the active processor can perform the burst transaction in verifying a memory coherency. Thus, the time required for verification can be remarkably reduced.